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EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	8

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/047,754	SRINIVASAN, VARADARAJAN	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,4,6 and 7*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received 14 January 2002, 27 June 2002, 21 January 2003, and 19 February 2004 have been considered. Please see attached PTO-1449(s).

Drawings

2. The drawings filed on 14 January 2002 have been approved by the Examiner.

Claim Rejections - 35 USC § 112

3. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 8 recites a global mask register coupled between a comparand storage element and the array of CAM cells. However, the specification does not describe the purpose or function of the global mask register, nor does the specification teach a coupling of the global mask register. In fact, the specification's sole reference to a global mask register merely specifies an undefined relationship to a comparand register (Page 12, paragraph 43, lines 11-12).

Lacking any description of function or structure, one skilled in the art would not be able to make and/or use the invention without undue experimentation.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 7, 9-10 and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713).

As in claim 1, Chow discloses a system comprising:

an array of CAM cells (Fig. 2, element 216);

a select circuit adapted to generate a selection criteria indicative of segments of input data provided to the system (Fig. 2, elements 204 and 206; page 4, paragraph 40); and

switch circuitry programmable to output a respective bit of the input data as a comparand bit for the array of CAM cells in response to the selection criteria (Fig. 2, element 210; page 4, paragraph 40), where it is noted that in view of the present application the terms reconfigurable and programmable are equivalent.

Chow does not teach that the selection criteria are a plurality of select signals, nor does Chow teach that the switch circuitry includes a plurality of programmable switch circuits each to output a bit in response to one of the select signals as required by claim 1.

Chow also does not explicitly teach a storage element between the switch circuits and the array of CAM cells for storing a comparand bit as required by claim 7.

Chow also does not teach a program circuit coupled to the switch circuits for programming the switch circuits as required by claim 9.

Baum teaches a crosspoint switch (i.e. crossbar) for reordering the fields of a database record that is controlled by a plurality of select signals generated by a select circuit (Fig. 17B, elements 1704, 1724 and 1725; column 30, lines 59-62; column 32, lines 16-18 and 42-48), where it readily apparent that the crosspoint switch contains a plurality of programmable switch circuits to output bytes in response to the select signals, and it is further noted that a byte comprises bits. Baum teaches that the field reordering is useful for picking subsets of fields for easier pattern matching (Column 30, lines 30-44).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the switch circuitry of Baum in the system of Chow, in order to pick subsets of fields for easier pattern matching.

Claim 4 is rejected according to the same rationale as for the rejection of claim 1 above.

Baum further teaches a storage buffer for staging the data being reordered through the switch (Fig. 17B, element 1728; column 32, lines 52-65; column 34, lines 30-34), where it is noted that buffer is coupled between the switch and the next processing stage, and that buffering of data in this manner is well known in the art as a means for pipelining operations in a system.

Regarding claim 7, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to store the data being reordered through the switch in a buffer coupled between the switch and the next processing stage (i.e. the array of CAM cells) as taught by Baum, in the system made obvious by the combination of Chow and Baum as applied to claim 1 above, in order to allow a pipelined operation of the system.

Baum also teaches a program circuit coupled to the switch circuits for programming the switch circuits in order to control the reordering of data through the switch (Fig. 17B, element 1724; column 32, lines 16-18 and 42-48).

Regarding claim 9, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to include a program circuit coupled to the switch circuits for programming the switch circuits as taught by Baum, in the system made obvious by the combination of Chow and Baum as applied to claim 1 above, in order to control the reordering of data through the switch as taught by Baum.

As in claim 10, Chow teaches that the position of a bit may change between the input data and the comparand data (Figs. 7A and 7B; page 5, paragraphs 49-51).

Claim 29 is rejected using the same rationale as for the rejection of claims 1 and 9 above, where it is noted that the program circuit of Baum (Fig. 17B, element 1724) programs the select circuit of Baum (Fig. 17B, element 1725), which in turn programs the switch (Fig. 17B, element 1704).

As to claim 30, the rationale derived from Chow and Baum in the rejection of claim 1 teaches:

receiving input data in a content addressable memory (CAM) apparatus having an array of CAM cells; and

selectively enabling programmed switch circuitry to filter at least one bit of the input data to generate at least on comparand bit for the array of CAM cells.

The combination of Chow and Baum as applied to claim 1 does not teach the following limitations as required by claim 30:

receiving a plurality of segments of input data;

receiving segment information indicative of which segment of the input data is received at any given time; and

enabling the programmed switch circuitry in response to the segment information.

Baum further teaches that a complete record of input data may be operated on sequentially by dividing the record into a number of quadwords (i.e. segments), and that the switch is enabled in response to segment information (i.e. i-counter value) indicating which segment of the input data is received at any given time (Figs. 17B, 18A-18C; column 34, lines 11-56). One skilled in the art would recognize that the sequential approach of Baum allows extraction and assembly operations to be performed on an input data record wider than the processing circuitry width, thereby trading off speed of computation for conservation of circuit area.

Regarding claim 30, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to receive a plurality of input data segments and to selectively enable the switch in response to segment information indicative of the particular segment of input data as taught by Baum, in the system of Chow and Baum as applied to claim 1 above, in order to trade off speed of computation for conservation of circuit area.

Claim 31 is rejected using the same rationale as for the rejection of claim 1 above.

As in claim 32, Chow discloses that the comparand is compared with data in the CAM (Page 4, paragraph 40), where the lookup operation in the CAM is understood to compare the input key (i.e. comparand) with data stored in the CAM.

6. Claims 2-3 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) as applied to claim 1 above, and further in view of Ninomiya (US 5,809,330).

Chow and Baum are relied upon for the teachings relative to claim 1 as above, where it is further noted that in the select circuit of Baum a counter provides input segment information to a decoder for generating the select signals to the crosspoint switch (Fig. 17B, elements 1725 and 1731; column 32, lines 59-65).

The combination of Chow and Baum does not teach that the select circuit comprises a memory element for storing programmed segment information, and a compare circuit to compare the programmed segment information with the input segment information to generate a select signal as required by claim 2.

The combination of Chow and Baum also does not teach that the memory element and compare circuit form a CAM cell as required by claim 3.

Ninomiya teaches a programmable decoder for generating select signals comprising memory elements for storing programmed information, and compare circuits to compare the programmed information with input information to generate a select signal (Fig. 4; column 9, line 59 to column 10, line 5). Ninomiya suggests that making the decoder programmable enables

the flexibility of changing the decoder behavior with a simple update to the stored program information (Column 3, lines 42-49).

Regarding claim 2, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the decoder of Ninomiya, to generate the select signals for the crosspoint switch in the system made obvious by the combination of Chow and Baum, in order to provide the flexibility of being able to change the decoding behavior as taught by Ninomiya.

Regarding claim 3, Ninomiya teaches memory elements paired with compare circuits. One of ordinary skill in the art would easily recognize that a memory element paired with a compare circuit comprises a CAM cell and therefore it would have been obvious to group these elements together in order to realize an area efficient design.

Claim 11 is rejected using the rationale as for the rejection of claim 2 above.

Claim 12 is rejected using the rationale as for the rejection of claim 4 above.

7. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) as applied to claim 1 above, and further in view of Reblewski (US Pub 2003/0131331).

Chow and Baum are relied upon for the teachings relative to claim 1 as above, where it is further noted that Chow teaches selecting bits individually from the input data (Figs. 7A-7B; page 5, paragraphs 49-51) while Baum teaches selecting bits as groups of bytes (Column 32, lines 42-49).

The combination of Chow and Baum does not teach an L-bit by L-bit switch with L select signals as required by claim 5.

Reblewski teaches a generic crossbar device where there is a one to one correspondence between the select signals, input data bits, output data bits (i.e. L-bit by L-bit switch with L select signals) (Figs. 1a –1b; page 1, paragraph 5, lines 1-7), where it is noted that the select signals are provided by memory elements corresponding to the switches. It is readily apparent that using a one to one correspondence between the select signals, input data bits and the output data bits enables fine-grained switching that allows manipulation of input data fields as small as one bit as taught by Chow.

Regarding claim 5, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use a one to one correspondence between select signals, input data bits and output data bits as taught by Reblewski, in the system made obvious by the combination of Chow and Baum, in order to enable the fine-grained switching that allows manipulation of single bit data fields as taught by Chow.

The combination of Chow, Baum and Reblewski as applied to claim 5 above, does not teach that the L input data bits are one of N segments of M input bits, where M is equal to N multiplied by L as required by claim 6. However, Baum further teaches that a complete record of input data (i.e. M input bits) may be operated on sequentially by dividing the record into a number (i.e. N segments) of quadwords (i.e. L input data bits) (Figs. 17B, 18A-18C; column 34, lines 11-56). One skilled in the art would recognize that the sequential approach of Baum allows extraction and assembly operations to be performed on an input data record wider than the processing circuitry width, thereby trading off speed of computation for conservation of circuit area.

Regarding claim 6, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to divide M input bits into N segments of L input data bits as taught by Baum, in the system of Chow, Baum and Reblewski as applied to claim 5 above, in order to trade off speed of computation for conservation of circuit area.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) as applied to claim 7 above, and further in view of Gandini (US 6,169,685).

Chow and Baum are relied upon for the teachings relative to claim 7 as above.

The combination of Chow and Baum does not teach a global mask register coupled to the comparand storage element and the array of CAM cells as required by claim 8.

Gandini teaches a CAM memory where a global mask register is coupled to a comparand register and an array of CAM cells in order to indicate comparand indifference conditions (Fig. 1, elements "RE" and "MA"; column 3, lines 36-46).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the global mask register as taught by Gandini, in the system of Chow and Baum, in order to indicate comparand indifference conditions as taught by Gandini.

9. Claims 13, 16, 19-20, 21, 24 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) and Kansal (US 6,374,326).

The rationale derived from the combination of Chow and Baum in the rejection of claim 1 above is incorporated herein for the teaching of a system comprising:

a CAM array block having R rows of L CAM cells, where R and L are integers greater than one;

a select circuit adapted to generate a plurality of select signals each indicative of a segment of input data provided to the CAM system; and

a switch circuit including a plurality of programmable switch circuits each programmable to output a respective bit of the input data as a comparand bit for a corresponding one of the CAM array blocks in response to one of the select signals.

The combination of Chow and Baum does not teach an integer plurality of the above system as required by claim 13.

Kansal teaches an integer plurality of CAM arrays for performing concurrent lookup operations (Figs. 2 and 3; column 1, line 66 to column 2, line 13). It is noted that although Kansal shows the comparand generation as a single functional unit (Figs. 2 and 3A, element 260), Kansal teaches the generation of a unique comparand for each lookup (Column 2, lines 14-23).

Regarding claim 13, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use a plurality of CAM lookup systems as taught by Kansal, where the CAM systems are embodied by the combination of Chow and Baum, in order to perform concurrent lookup operations as taught by Kansal.

Claim 21 is rejected using the same rationale as for the rejection of claim 13 above, further noting that Kansal teaches that the plurality of CAM arrays may be comprised of both individual CAM arrays and subdivisions of a single CAM array (Figs. 2 and 3; column 3, lines 25-58).

Claims 16 and 24 are rejected using the same rationale as for the rejection of claim 4 above.

Claims 19 and 27 are rejected using the same rationale as for the rejection of claim 9 above.

Claims 20 and 28 are rejected using the same rationale as for the rejection of claim 10 above.

10. Claims 14-15 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) and Kansal (US 6,374,326) as applied to claims 13 and 21 above, and further in view of Ninomiya (US 5,809,330).

Chow, Baum and Kansal are relied upon for the teachings relative to claims 13 and 21 as above.

Claims 14 and 22 are rejected using the same rationale as for the rejection of claim 2 above.

Claims 15 and 23 are rejected using the same rationale as for the rejection of claim 3 above.

11. Claims 17-18 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) and Kansal (US 6,374,326) as applied to claims 13 and 21 above, and further in view of Reblewski (US Pub 2003/0131331).

Chow, Baum and Kansal are relied upon for the teachings relative to claims 13 and 21 as above.

Claims 17 and 25 are rejected using the same rationale as for the rejection of claim 5.

Claims 18 and 26 are rejected using the same rationale as for the rejection of claim 6.

12. Claims 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ninomiya (US 5,809,330) in view of Lindholm (US 5,890,005).

As in claim 33, Ninomiya discloses a method comprising:

receiving first data on an input bus of a device for performing a write operation (Figs. 3 and 4, "DATA BUS"; column 9, lines 1-13); and

receiving second data on an input bus of a device for performing a compare operation (Figs. 3 and 4, "ADDRESS BUS"; column 9, lines 1-13).

The rationale derived from Ninomiya in the rejection of claim 3 above is incorporated herein for the teaching that the memory element and compare circuit pairs in Fig. 4 of Ninomiya comprise a CAM cell.

Ninomiya does not teach that the first and second data are received on the same bus as required by claim 33.

Lindholm teaches that a reduction in the number of data bus interconnections in a processing system can be reduced by multiplexing address and data information onto a single bus (Fig. 1A, element 1A; column 4, lines 43-45).

Regarding claim 33, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to multiplex the address and data on a single bus as taught by Lindholm, in the method of Ninomiya, in order to reduce the number of data bus interconnections as taught by Lindholm.

Regarding claim 34, it is readily apparent that the first and second data in the combined method of Ninomiya and Lindholm is time multiplexed, otherwise there would be contention on the bus.

As in claim 35, the first data in Ninomiya is transmitted to read/write circuitry (Fig. 4; column 9, line 59 to column 10, line 5).

As in claim 36, the second data in Ninomiya is transmitted to a filter circuit (Fig. 4; column 9, line 59 to column 10, line 5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabh 3/8/04

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